Notice of Allowability	Application No.	Applicant(s)	
	09/839,671	MATSUI, KATSUAKI	
	Examiner	Art Unit	
	Jeffrey R. West	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the Amendment filed October 13, 2005*.

2. ☒ The allowed claim(s) is/are *21-23 and 44*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Allowable Subject Matter

1. Claims 21-23 and 44 are considered to be allowable over the cited prior art for the following reasons:

Japanese Publication No. 2000-030492 to Kurihara discloses a semiconductor device having an access time measuring test mode comprising a circuit block to which an input signal is input at a timing in accordance with an input clock, and which outputs an output signal having a value corresponding to said input signal (0001 and Figures 1 and 2), a first signal path for guiding a test input signal, which has been supplied to a first terminal, from said first terminal to a signal input terminal of said circuit block ("ADO" in Figure 1), a second signal path for guiding a test clock, which has been supplied to a second terminal, from said second terminal to a clock input terminal of said circuit block ("CLK" in Figure 1), a third signal path for guiding a test output signal, which has been output from a signal output terminal of said circuit block, from said signal output terminal to a third terminal ("DO" through "2" and "TDO" in Figure 1), a fourth signal path for guiding said test clock, which is input to said clock input terminal, from said clock input terminal to a fourth terminal ("CLK" through "3" and "4" and "TCK" in Figure 1), wherein said third and fourth signal paths are formed so that wiring delay time of said third and fourth signal paths are substantially equal (i.e. the delay of flop-flop circuit "2" is controlled to be the same as the amount of delay in the delay circuit "4") (0014).

U.S. Patent No. 5,661,685 to Lee et al. teaches a programmable logic device with a configurable power supply including means for accessing signals at a pad (column 9, line 63 to column 10, line 3).

U.S. Patent No. 5,337,321 to Ozaki teaches a scan path circuit including means for testing a circuit block including a first signal path for guiding a test input signal to a signal input terminal of the circuit block (input to "D" of circuit block "22", Figure 2), a second signal path for guiding a test clock to a clock input terminal of the circuit block ("37", Figure 2), a third signal path for guiding a test output signal from a signal output terminal of the circuit block ("33", Figure 2), and a fourth signal path for guiding the test clock from the clock input terminal (path from branch of "37" to selector "27", Figure 2).

Ozaki also teaches that said fourth signal path has provided therein a first selector ("27", Figure 2), responsive to a mode of a selection signal (column 3, lines 9-14), that selectively supplies a prescribed signal or said test clock directly to a neighboring device (column 3, lines 15-27), wherein an output terminal of said first selector and said neighboring device are directly connected by a first wiring ("38", Figure 2).

Ozaki also teaches that said third signal path has provided therein a second selector ("26", Figure 2) which during a normal operation supplies a second prescribed signal other than said test output signal to a neighboring device and which during a test operation supplies said test output signal to said neighboring device (column 3, lines 2-14) and wherein an output terminal of said second selector

and said neighboring device are directly connected by a second wiring (input to "D" of circuit block "23", Figure 2).

Ozaki also teaches that the first signal path has provided therein a third selector ("25", Figure 2) which during the normal operation supplies an output signal from a preceding circuit block to said test signal input terminal of said circuit block and which during the test operation supplies said test input signal to said signal input terminal of said circuit block (column 3, lines 2-14). Ozaki also teaches that said second signal path has provided therein a third/fourth selector ("28", Figure 2) which during the normal operation supplies a normal clock to said clock input terminal of said circuit block and which during the test operation supplies said test clock to said clock input terminal of said circuit block (column 3, lines 15-27).

As noted above, the cited prior art teaches many of the features of the claimed invention. The invention of Kurihara, specifically, teaches a semiconductor access time measurement circuit, however, the invention of Kurihara specifically includes delay circuitry and/or flip-flop circuitry on the third and fourth signal paths. Therefore, any combination with Kurihara to include selection circuits on the third and fourth signal paths would also include such circuitry, thereby teaching away from the invention as claimed requiring a first wiring that directly (i.e. without any intervening component) connects said clock input terminal of said circuit block to an input terminal of said first selector and a second wiring that directly (i.e. without any intervening component) connects an output terminal of said first selector to said

fourth pad and a third wiring that directly (i.e. without any intervening component) connects said signal output terminal of said circuit block to an input terminal of said second selector, and a fourth wiring that directly (i.e. without any intervening component) connects an output terminal of said second selector to said third pad. These circuits are also considered to be critical to the invention of Kurihara as they are required to carry out the measuring functionality, and therefore any proposed modification to remove such circuitry would be non-obvious since it would destroy the operation of Kurihara.

Therefore, while the cited prior art teaches many of the features of the claimed invention, the cited prior art does not teach or suggest, in combination with the other claimed limitations for a semiconductor device having an access time measuring test mode, a third signal path for guiding a test output signal, which has been output from a signal output of a circuit block, from the signal output terminal to a third pad, a fourth signal path for guiding a test clock, which is input to a clock input terminal, from the clock input terminal to a fourth pad, wherein said third and fourth signal paths are formed so that wiring delay time of the third and fourth signal paths are substantially equal and wherein said fourth signal path has provided therein a first selector, responsive to a mode of a selection signal, that selectively supplies a prescribed signal or said test clock directly to said fourth pad, a first wiring that directly (i.e. without any intervening component) connects said clock input terminal of said circuit block to an input terminal of said first selector and a second wiring that directly (i.e. without any intervening component) connects an output terminal of said

first selector to said fourth pad and wherein said third signal path has provided therein a second selector which during a normal operation supplies a second prescribed signal other than said test output signal to said third pad and which during a test operation supplies said test output signal to said third pad, a third wiring that directly (i.e. without any intervening component) connects said signal output terminal of said circuit block to an input terminal of said second selector, and a fourth wiring that directly (i.e. without any intervening component) connects an output terminal of said second selector to said third pad.

The following prior art references are also considered to be relevant to the claimed invention but fail to teach or suggest the claimed invention for the reasons provided above:

U.S. Patent No. 6,424,583 to Sung et al. teaches a system for measuring access time of embedded memories.

U.S. Patent No. 6,327,218 to Bosshart teaches an integrated circuit time delay measurement apparatus.

JP Patent Application Publication No. 02-184048 to Sato et al. teaches a semiconductor integrated circuit having a built-in memory with capability to measure an address access time.

U.S. Patent No. 6,512,707 to Miura et al. teaches a semiconductor integrated circuit device allowing accurate evaluation of access time of a memory core contained therein and an access time evaluating method.

U.S. Patent No. 6,266,749 to Hashimoto et al. teaches an access time measurement circuit and method.

JP Patent Application Publication No. 61-016615 to Kato teaches a phase synchronizing circuit with the capability of measuring semiconductor propagation delay.

U.S. Patent No. 5,198,999 to Abe et al. teaches a serial input/output semiconductor memory including an output data latch circuit.

U.S. Patent No. 6,948,106 to Porterfield teaches a method and system for partial-scan testing of integrated circuits.

U.S. Patent No. 6,393,592 to Peeters et al. discloses scan flop circuitry and methods for making the same comprising a circuit block for connection to previous circuit blocks in a scan chain (column 4, lines 20-24) including a circuit block in which an input signal is input at a timing in accordance with an input clock and which outputs an output signal having a value corresponding to said input signal comprising a first signal path for guiding a test input signal to a signal input terminal of the circuit block, a second signal path for guiding a clock to a clock input terminal of the circuit block, and a third signal path for guiding an output signal (Figure 3). Peeters also discloses a selector on the first signal path which, during normal operation, supplies an output signal from a preceding circuit block to the input terminal of the circuit block and which during a test operation supplies the test input signal to the signal input terminal of the circuit block as well as a selector on the second signal path which, during normal operation supplies a normal clock to the

input terminal of the circuit black and during a test operation supplies a test clock to the clock input terminal of the circuit block (Figure 3 and column 4, lines 21-39). Peeters also discloses the conventional method of receiving and outputting the signals via test pads (Figure 1B, "SI", "CLK", and "SO").

U.S. Patent No. 6,615,380 to Kapur et al. teaches dynamic scan chains and test pattern generation methodologies comprising a plurality of circuit blocks connected in a scan chain wherein the path for guiding the test output signal from a signal output terminal includes a selector which supplies a test signal during testing and a normal output during normal operation (Figure 4 and column 2, lines 24-33).

2. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey R. West whose telephone number is (571)272-2226. The examiner can normally be reached on Monday through Friday, 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (571)272-2216. The fax phone number

for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jrw
November 14, 2005

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